MORNSUN®

TD551S485H
SOIC16 package isolated RS485 Half Duplex Transceiver

Features

- Ultra-small, ultra-thin, chip scale SOIC16 package
- Compliant with TIA/EIA-485-A standard
- Power supply 5.0V
- Integrated efficient isolation power supply with overload and short circuit protection
- I/O power supply range supports 5V microprocessors
- High isolation to 6000VDC/4000VAC
- Bus-Pin ESD protection up to 15kV(HBM)/±4kV(Contact discharge)
- Baud rate up to 10Mbps
- High common mode transient immunity 180kV/μs (typical value)
- Nanosecond level communication delay
- 1/8 unit load—up to 256 nodes on a bus
- Bus fail-safe
- Bus driver short circuit protection
- Industrial operating ambient temperature range: -40℃ to +125℃

Package

Applications

- Industrial Automation
- Building Automation
- Smart Electricity Meter
- Remote Signal Interaction, Transmission

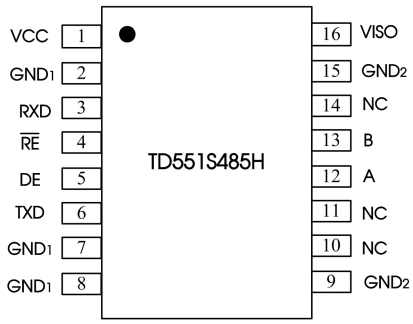
Functional Description

TD551S485H is a half-duplex enhanced transceiver designed for RS-485/RS-422 data bus networks, has high electromagnetic immunity and low radiation characteristics which is fully compliant with TIA/EIA-485-A standard and is suitable for data transmission of up to 10Mbps. Receivers have an exceptionally high input impedance, which places only 1/8 of the standard load on a shared bus and up to 256 transceivers.

The TD551S485H device has high insulation capacity, which helps to prevent noise and surges on the data bus or other circuits from entering the local grounding terminal, thereby interfering or damaging sensitive circuits. High CMTI capability can ensure the correct transmission of digital signals. On the basis of traditional IC, the focus is on strengthening the reliability design of A, B pins, including driver overcurrent protection and enhanced ESD design. The A, B ports can withstand ESD up to ±15kV (HBM) and ±4kV (contact discharge).

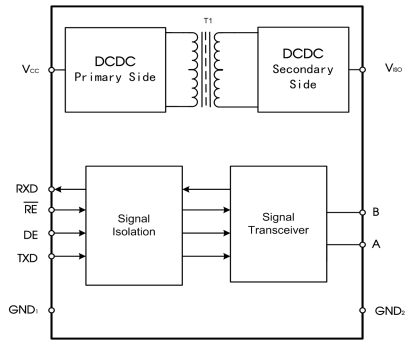
Contents

Pin Connection



Note：Pin7, Pin8 GND_1 are connected, Pin2 GND_1 is not internally connected with other GND_1; Pin9 and Pin15 GND_2 are internally disconnected.

Internal Block



Function Table

Letter	Description
H	High-Level
L	Low-Level
X	Unrelated
Z	High Impedance

Table 1. Driver Function table

TXD	DE	Output	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

Table 2. Receiver Function table

$V_{ID} = (V_A - V_B)$	$\overline{RE}$	RXD
–0.02 V ≤ V_{ID}	L	H
–0.22 V < V_{ID} < –0.02V	L	Uncertainty
V_{ID} ≤ –0.22 V	L	L
X	H	Z
Open circuit	L	H

Note:

① When driving status, the DE and RE pins are connected to a high level;

② When receiving status, the DE and RE pins are connected to a low level;

Pin Descriptions

Pin Number	Pin Name	Pin Functions
1	V_{CC}	Power supply. By using 0.1uF and 10uF ceramic capacitance ground (GND1).
2	GND_1	Logic side reference ground.
3	RXD	Receiver Output Data.
4	$\overline{RE}$	Receiver enable input. When $\overline{RE}$ is low, if (A − B) ≥ −20 mV, then RXD = high. if (A − B) ≤ −220 mV, then RXD = low.
5	DE	Driver enable input. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode.
6	TXD	Driver Input.
7	GND_1	Logic side reference ground. The pin needs to be connected to pin2 in application.
8	GND_1	Logic side reference ground. The pin needs to be connected to pin2 in application.
9	GND_2	Bus side reference ground.
10	NC	No Function Pin, Dangling.
11	NC	No Function Pin, Dangling.
12	A	RS485 Bus A wire pin.
13	B	RS485 Bus B wire pin.
14	NC	No Function Pin, Dangling
15	GND_2	Bus side reference ground. The pin needs to be connected to pin9 in application.
16	V_{ISO}	Isolate the power output. Close to this pin, 0.1uF and 10uF ceramic capacitors must be connected to the bus side reference ground (GND_2).

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (Unless otherwise specified).

Parameters	Unit
Supply voltage	-0.5V to +6V
Output voltage Vin	-0.5V to V_{CC}+0.5V
Output current IO	-10mA to +10mA
Junction temperature TJ	< 150℃
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Important: Exposure to absolute maximum rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage. All voltage values are based on the reference ground(GND) maximum voltage not exceeding 6V.

Recommended Operating Conditions

Symbol	Recommend an operate condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_I	A, B pin voltage	-7	--	12	
V_{IH}	High-level input voltage	2	5.0	5.5	
V_{IL}	Low-level input voltage	0	--	0.8	
T_A	Operating temperature range	-40	25	125	℃
DR	Signaling rate	--	--	10	Mbps

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver						
$\|V_{OD}\|$	Common mode output voltage	No load	4.5	--	5.2	V
		RL=60 Ω	1	--	3	
$\|V_{OD3}\|$	Absolute value of differential output voltage	No load	4.5	--	--	V
		RL=60 Ω	1.5	--	--	
ΔV_{OD}	Δ$\|V_{OD}\|$ for complementary output states	No load, Figure 7	-0.2	--	0.2	V
V_{IH}	high level output voltage	TXD, DE, $\overline{RE}$	2	5	5.5	V
V_{IL}	low level output voltage	TXD, DE, $\overline{RE}$	0	--	0.8	V
I_A	Driver short-circuit current		--	±100	±200	mA
CMTI	Common mode transient immunity	V_{CM} = 1200V; Figure 12	--	180	--	kV/μS
Receiver						
$V_{IT(+)}$	Positive differential input threshold voltage	−7 V ≤ V_{CM} ≤ +12 V	--	--	–20	mV
$V_{IT(-)}$	Negative differential input threshold voltage	−7 V ≤ V_{CM} ≤ +12 V	–220	--	--	mV
Vhys	Hysteresis voltage (V_{IT+} – V_{IT-})	−7 V ≤ V_{CM} ≤ +12 V		30	--	mV
V_{OH}	RXD high level output voltage		Vcc − 0.4	4.8		V
V_{OL}	RXD low level output voltage		0	0.2	0.4	V
I_A	Receiver output current		--	--	±100	mA
I_{IH}	Input high-level leakage current RE	V_{IH}=2V	--	--	20	uA
I_{IL}	Input low-level leakage current RE	V_{IH}=0.8V	-20	--	--	
R_{ID}	Differential input resistance(A, B)	−7 V ≤ V_{CM} ≤ +12 V	96	--	--	kΩ
Power supply and safeguard characteristic						
V_{ISO}	Isolated power output voltage	V_{CC}=5V, distribution unloaded, signal fully loaded	4.80	5.06	5.30	V
EMI	Conducted Disturbance	CISPR32/EN55032 CLASS B; Figure 16				
	Radiated Disturbance	CISPR32/EN55032 CLASS A; Figure 16				
ESD	HBM Mode	A, B ports	--	--	±15	kV
	Contact discharge mode	A, B ports	--	--	±4	kV
V_{IO}	Insulate voltage	Input-Output, Leakage current<1mA Rise time 3s, Fall time 1s Test time 1s	--	--	6000	VDC
			--	--	4000	VAC
		Input-Output, Leakage current<1mA Rise time 3s, Fall time 1s Test time 60s	--	--	5000	VDC
			--	--	3500	VAC
R_{IO}	Insulate impedance		1	--	--	GΩ

Transmission Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
-	Data rate	Duty40% ~ 60%	--	--	10	Mbps
T_{PHL},T_{PLH}	Driver propagation delay	R_L=60Ω, C_{L1}=C_{L2}=50pF Figure8 Figure11	--	50	90	ns
$\|T_{PHL}$-$T_{PLH}\|$	Driver skew ($\|T_{PHL}$ - $T_{PLH}\|$)		--	--	25	ns
T_R,T_F	Driver rise/fall time		--	6	25	ns
t_{PZH}/ t_{PZL}	Drive off enable propagation delay		--	--	80	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PHZ}/ t_{PLZ}	Drive Enable Propagation Delay		--	50	80	ns
T_{PHL},T_{PLH}	Receiver propagation delay	R_L=60Ω C_L = 15pF, Figure9	--	70	110	ns
|T_{PHL}-T_{PLH}|	Receiver propagation delay		--	--	25	ns
T_R,T_F	Receiver rise/fall time	R_L=60Ω C_{L1}=C_{L2}=50pF Figure9 Figure10	--	2	10	ns
t_{PLH}	Receive off enable propagation delay, Output low-level to high-level time		--	--	80	ns
t_{PHL}	Receive enable propagation delay time, Output high-level to low-level time		--	--	80	ns

Physical Specifications

Parameters	Value	Unit
Weight	0.4(Typ.)	g

Parameter testing circuit

Note: Test condition load capacitance includes test probe and fixture parasitic capacitance (no special instructions). The rising and falling edges of the test < 6ns. frequency 100kHz. duty50%. resistance Z_O = 54Ω.

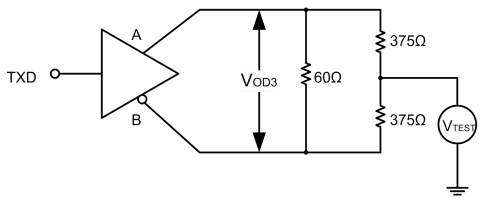


Figure 6. Common mode output test circuit

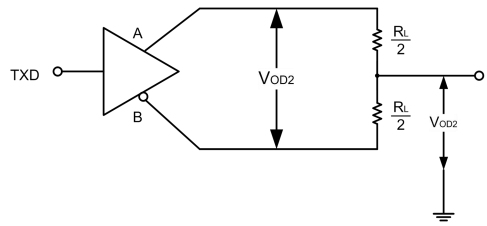
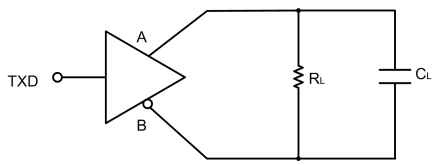


Figure 7. Differential output test circuit



Note: CL includes parasitic capacitance of fixtures and instruments

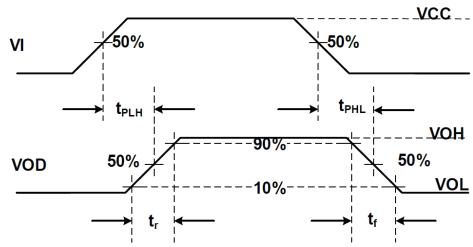
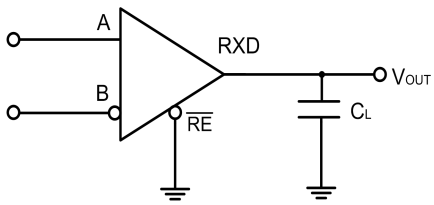


Figure 8. Drive propagation delay test circuit and wave forms



Note: CL includes parasitic capacitance of fixtures and instruments

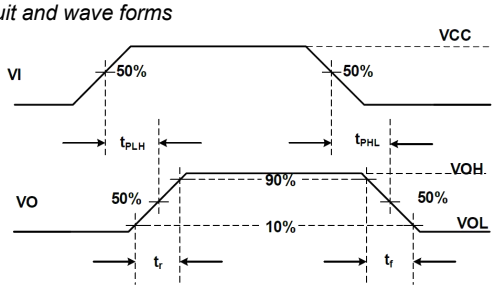
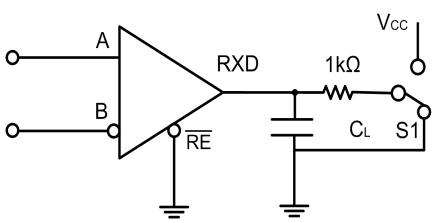


Figure 9. Receiver propagation delay test circuit and wave forms



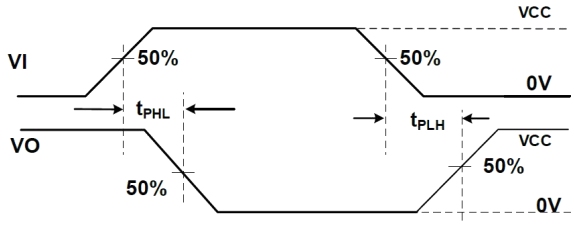
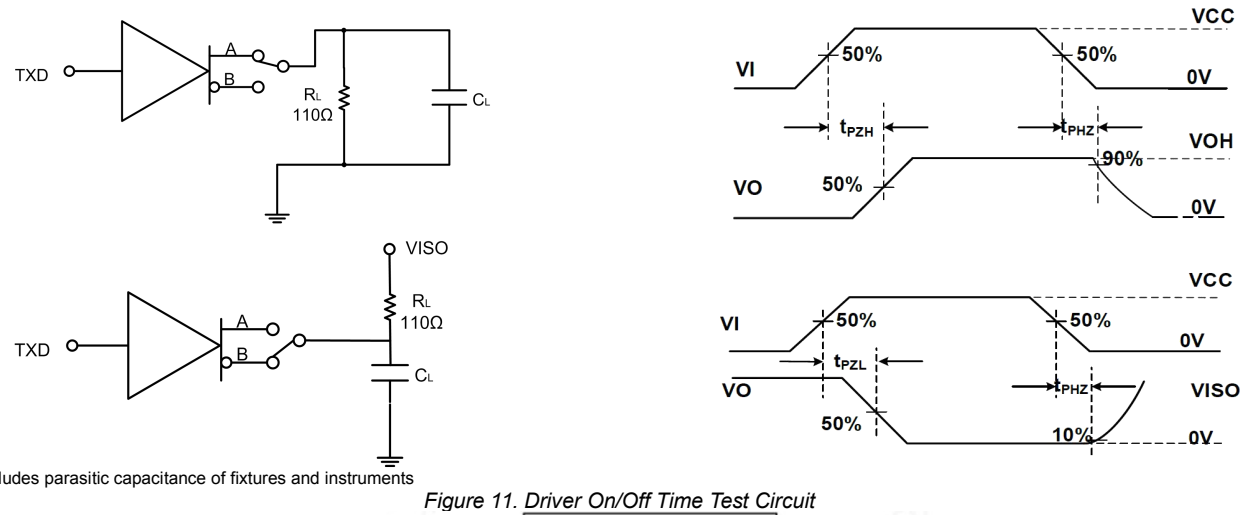


Figure 10. Receiving on/off time test circuit



Note: CL includes parasitic capacitance of fixtures and instruments

Figure 11. Driver On/Off Time Test Circuit

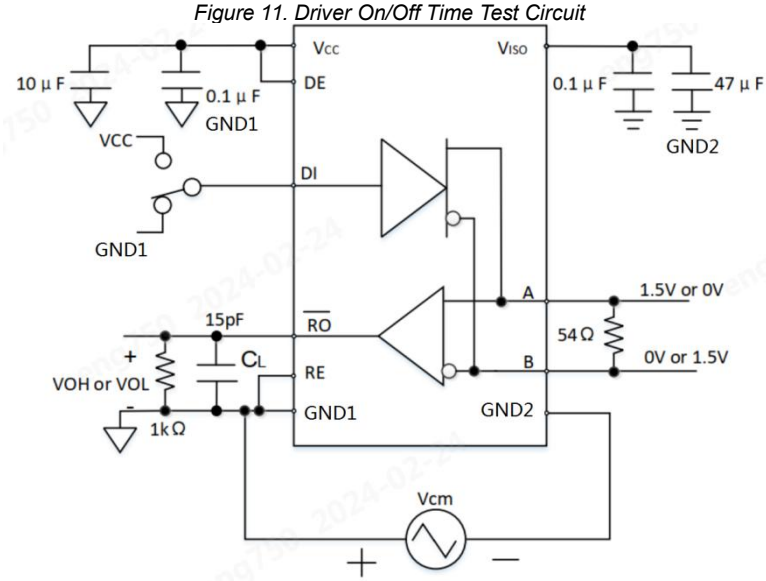


Figure 12. CMTI Test Circuit

Detailed Description

TD551S485H is a half-duplex enhanced RS-485 isolated transceiver with isolated power supply. In addition to an isolated power supply, each transceiver contains a drive and a receiver. The transceiver has a standby bus failure protection function to ensure that the receiver output is high when the receiver input is open, short, or when the bus is idle.equipped with failure safety, overcurrent protection, and overheating protection functions.

Bus failure protection: When the receiver input is short circuited or open, and all drivers hanging on the terminal matching transmission line are disabled (idle), the TD551S485H product can ensure that the receiver output logic is high. This is achieved by setting the input threshold of the receiver to -220mV and -20mV, respectively. If the input voltage (A-B) of the differential receiver is ≥ -20mV, RO is the logic high level; If the voltage (A-B) is ≤ -220mV, RO is the logic low level. When all transmitters connected to the terminal matching bus are disabled, the differential input voltage of the receiver will be pulled to 0V through the terminal resistor. Based on the receiver threshold, a logic high level with a minimum noise tolerance of -20mV can be achieved- The threshold voltage from 220mV to -20mV is in accordance with EIA/TIA-485 standards.

The bus load capacity (256 point): standard RS485 receiver input impedance is defined as 12kΩ (unit load). A standard RS485 driver can drive at least 32 load units. TD551S485H bus receiver designed by 1/8 unit load, the input impedance is greater than 96kΩ. As a result, the bus allows access to more transceivers (up to 256). TD551S485H can also be mixed with the standard RS485 transceiver with 32 unit loads (cumulative receiver load cannot exceed 32 units).

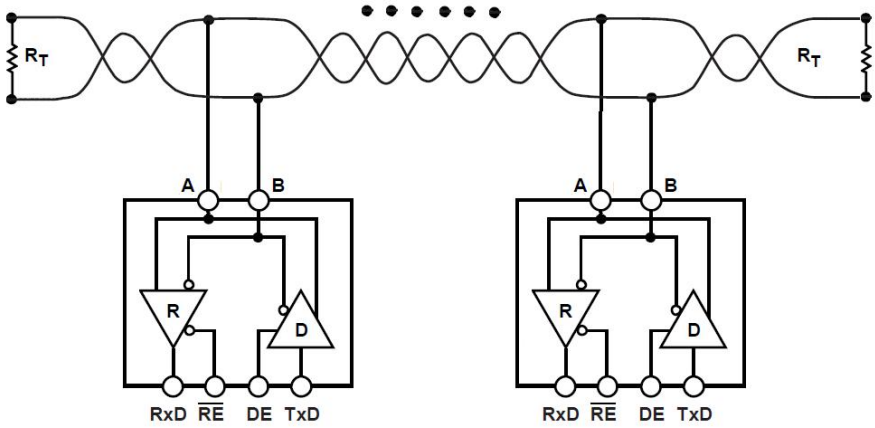


Figure13.Typical application circuit (half-Duplex Network Topology)

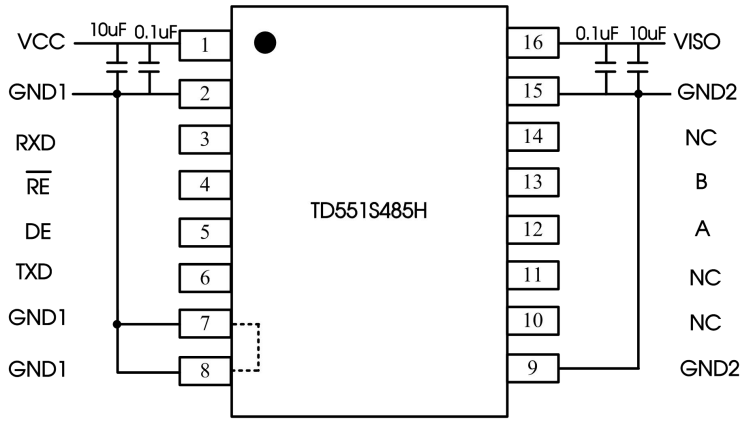


Figure 14. Typical Application Diagram

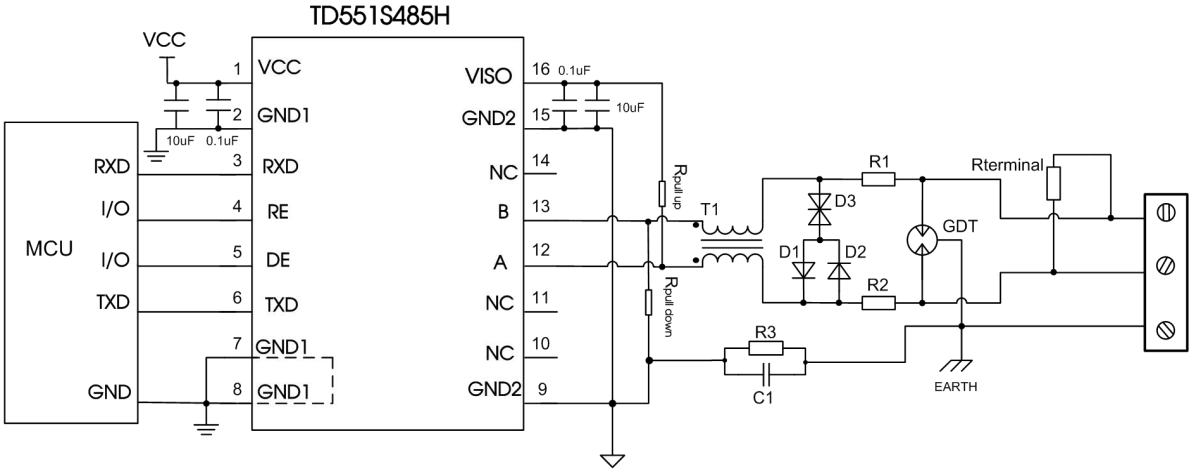


Figure 15. Port protection circuit for harsh environments

Parameter Description:

Component	Recommended part, value	Component	Recommended part, value
R3	1MΩ	R1, R2	2.7Ω/2W
C1	1nF, 2kV	D1, D2	1N4007
T1	ACM2520-301-2P	D3	SMBJ8.5CA
GDT	B3D090L	$R_{terminal}$	120Ω

As the modules internal A / B lines come with its own ESD protection, which generally satisfy most application environments without the need for additional ESD protection devices. For harsh and noisy application environments such as motors, high voltage/current switches, lightning and similar however, we recommended that the user protects the module's A / B lines with additional measures and external components such as TVS tube, common mode inductors, Gas discharge tube, shielded twisted pair of wires with the same single network Earth point. Figure 15 shows our recommended circuit diagram for such type of applications with components and values given in the table above. This recommendation is for reference only and may have to be adapted accordingly with appropriate component values in order to match the actual situation and application.

Note 1: Select the $R_{terminal}$ according to the actual application.

Note 2: When using the port protection circuit, you need to slow down the baud rate.

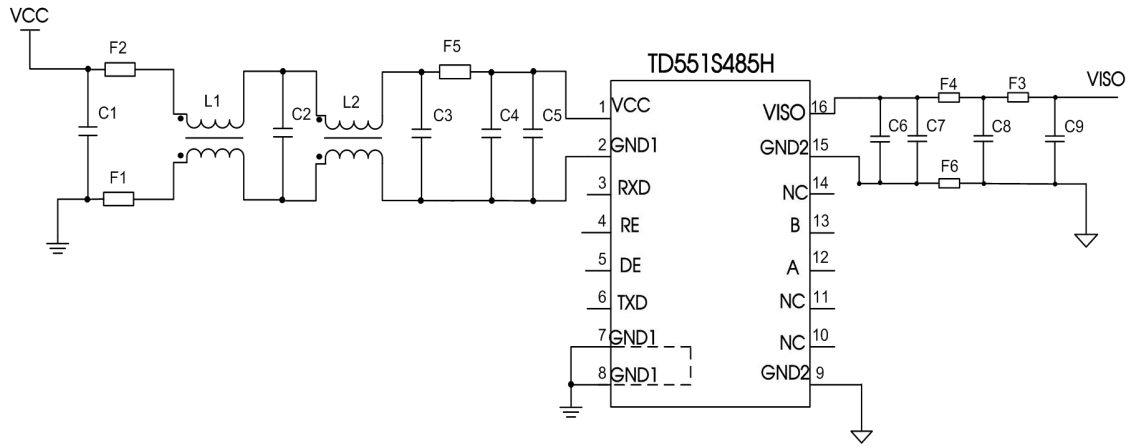


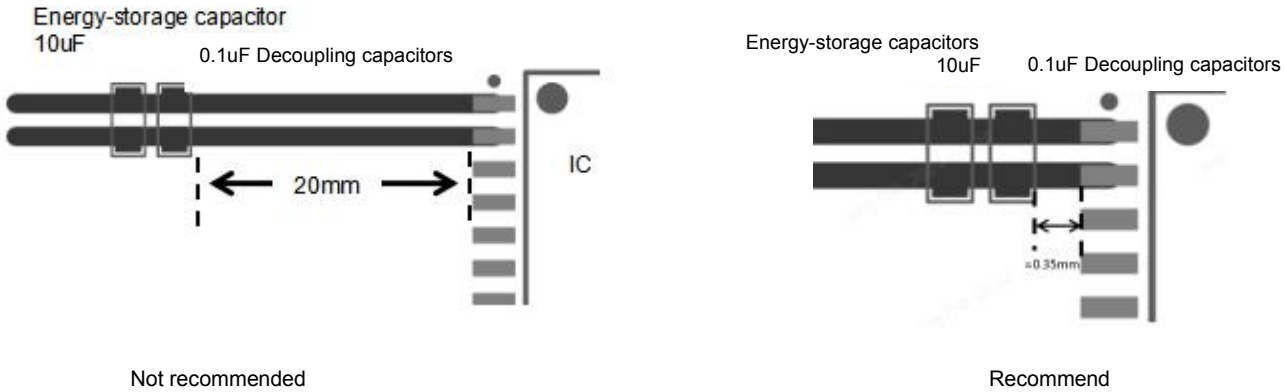
Figure 16.circuit for EMI

Parameter Description:

Component	Recommended part, value
F1, F2, F3, F4, F5, F6, F7	UP1608U601-1R3TF (DCR 0.15Ω Max)
C1, C2, C3, C4, C7, C8, C9	10uF
C5, C6	0.1uF
L1	Nickel core: 138uH
L2	Nickel core: 78uH
R1, R2, R3, R4	120Ω

PCB design description:

1. The decoupling capacitors and energy storage capacitors of VCC and GND1, VISO and GND2 should be placed as close to the chip pins as possible to reduce the loop area and parasitic inductance of PCB wiring. Generally, it should be controlled within 0.35mm. The decoupling capacitor is placed near the chip, and the energy storage capacitor is placed on the outside. As shown in Figure 17-1.

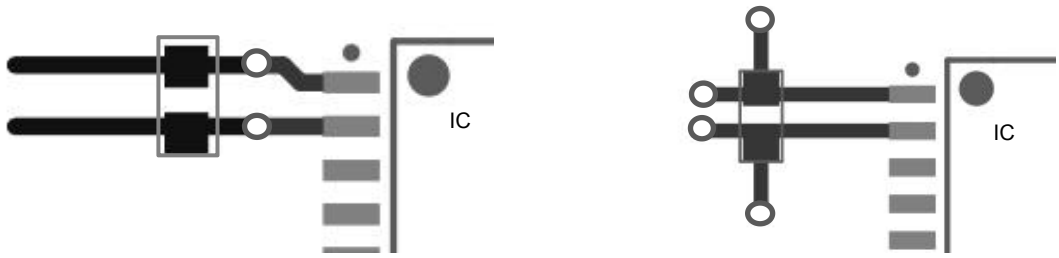


Not recommended

Recommend

Figure 17-1

2. When wiring, the power line width should be designed to be at least 0.5mm.
3. When it is necessary to place vias in the power supply line and ground wire, the position of the vias should be on the outer side of the capacitor relative to the chip pins, rather than between the capacitor and the chip, as shown in Figure 17-2 to reduce the impact of parasitic inductance in the vias.



Not recommended

Recommend

Figure 17-2

Recommendations

① The product does not support hot-plugging.

② TXD external inputs should have pull-up resistors added as appropriate if drive capability is insufficient.

③ In order to maintain the bus idle stability, it is necessary to pull up A to VISO and pull down B to GND2 in at least one node at the bus end, while the pull-up and down resistors of the overall network have a parallel value of 380Ω~420Ω (0.2W).

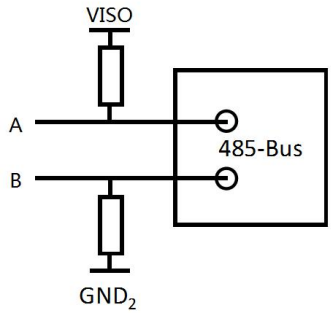


Figure 18. Typical Pull-Up and Pull-Down Resistor Connections

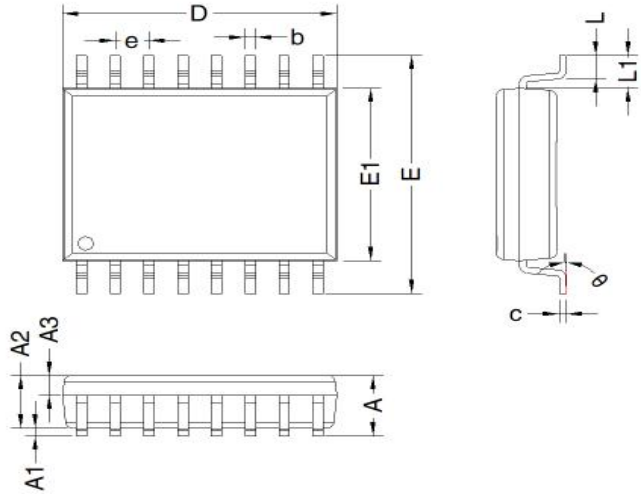
④ High when the product's internal DE and TXD are overhanging, and low when $\overline{RE}$ is built-in overhanging.

Ordering Information

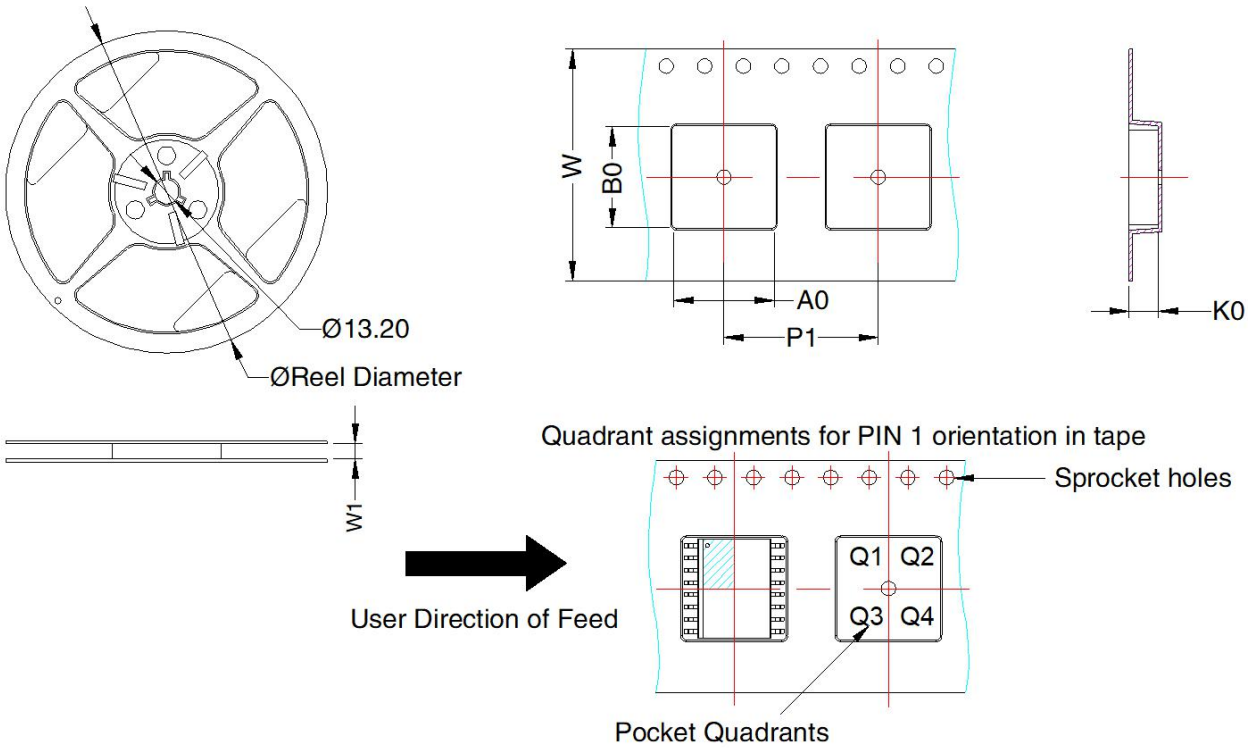
Part number	Package	Number of pins	Product marking	Tape & Reel
TD551S485H	SOIC	16	TD551S485H	340/REEL

Package Information

THIRD ANGLE PROJECTION



Max	Unit (mm)	
	Min	Max
A	–	2.65
A1	0.10	0.30
A2	2.25	2.35
A3	0.97	1.07
b	0.35	0.43
c	0.24	0.29
D	10.20	10.40
e	1.27 BSC	
E	10.10	10.50
E1	7.40	7.60
L	0.55	0.85
L1	1.40 BSC	
θ	0°	8°



Package Type	Pin	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SOIC–16	16	340	180.0	16.4	10.74	10.65	3.05	16.0	16.0	Q1

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